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EXAMINER	
GANDHI, DIPAKKUMAR B	
ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/673,211	MONTAGNE ET AL.	
	Examiner	Art Unit	
	DIPAKKUMAR GANDHI	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) *9,11 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8,10,12-20 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Response to Amendment

1. The amendment filed on 3/20/2008 has been entered.

2. Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1, 2, 3, 4, 5, 6, 7, 8, 10, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al. (Testing and Diagnosis of Interconnect Faults in Cluster-based FPGA Architectures, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 21, Issue 11, November 2002, Pages 1337-1343) in view of Venkatesan (Modelling Feedback Control Adjustment to Control Output Product Quality, Proceedings of American Control Conference, May 2002, vol. 6, Pages 5049-5053).

As per claim 1, Harris et al. teach a method for testing configurable logic blocks in an emulation system, the method comprising steps of: configuring a first set of configurable logic blocks to be first testing circuitry; operating the first set to test a second set of configurable logic blocks; configuring each configurable logic block of the second set to respond with a deterministic output to an N-bit input, wherein

the configuring the first set includes configuring a configurable logic block of the first set as a verifier to verify a responsive output of the second set organized into M groups of configurable logic blocks ("In this paper, an FPGA fault test and diagnosis approach is described that performs built-in self-test (BIST) on a cluster-based FPGA device. During the testing process, a portion of the FPGA is configured as test generation and response circuitry for a cluster under test. As individual logic clusters and surrounding routing resources are verified, they subsequently may be used to perform testing on remaining, untested clusters. To demonstrate the approach, we present a technique to generate FPGA test configurations to detect and diagnose pairwise bridging interconnect faults", page 1337, col. 2, paragraph 3,Harris et al. "In each configuration, FPGA circuitry dedicated as BIST logic will perform test generation and response analysis to test non-BIST FPGA circuitry. To accomplish BIST, we use the test structure presented in [10] in which the FPGA is configured as many independent BISTER's structures, shown in Fig. 3. Each BISTER is composed of a test pattern generator (TPG), an output response analyzer (ORA), and two blocks under test (BUTs). The TPG is simply a counter which applies an exhaustive test sequence to the BUTs. Each BUT is a single tile in the FPGA which is being tested. The ORA is a comparator which sets the Pass/Fail flip-flop to "1" if the outputs of both BUTs do not agree. Each BISTER will be implemented as a rectangular block of tiles, and many BISTERs will be implemented on the FPGA to cover the tile array. The number of tiles in a BISTER will depend on the number of tiles needed to implement the TPG and ORA logic", fig. 3, page 1338, col. 2, paragraphs 2-3, Harris et al.).

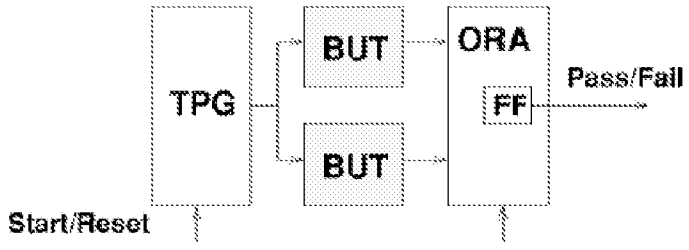

Fig. 3. BISTER test structure.

However Harris et al. do not explicitly teach that the verifier is configured to accept its own output as one bit of the N-bit input, wherein, upon the output of the verifier being a failure indicator, the verifier is configured to maintain the failure indicator for the test.

Venkatesan in an analogous art teaches that this paper describes a method to model feedback control adjustment to control the quality of products at the output of a continuous process. The method takes into consideration situations in which the product quality mean is on target and not on target by assigning suitable probabilities for the respective situations (abstract, Venkatesan).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Harris et al.'s publication with the teachings of Venkatesan by including additionally that the verifier is configured to accept its own output as one bit of the N-bit input, wherein, upon the output of the verifier being a failure indicator, the verifier is configured to maintain the failure indicator for the test. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to keep a steady output value of the failure indicator.

- As per claim 2, Harris et al. and Venkatesan teach the additional limitations.

Harris et al. teach configuring the second set to be second testing circuitry; and operating the second set to test the first set ("Each BISTER will be implemented as a rectangular block of tiles, and many BISTERs will be implemented on the FPGA to cover the tile array. The number of tiles in a BISTER will depend on the number of tiles needed to implement the TPG and ORA logic. It is important to notice that the tiles which are dedicated to the TPG and ORA logic are not completely tested. In order to guarantee testing of all tiles, the FPGA will be reconfigured to shift the BISTERs across the entire array as shown in Fig. 4. Over the course of several reconfigurations, all tiles will be tested by acting as a BUT in a BISTER", page 1338, col. 2, paragraphs 3-4, Harris et al.).

- As per claim 3, Harris et al. and Venkatesan teach the additional limitations.

Harris et al. teach configuring a third set of configurable logic blocks to be second testing circuitry; and operating the third set, concurrently with the first set, to test a fourth set of configurable logic blocks ("Each BISTER will be implemented as a rectangular block of tiles, and many BISTERs will be

implemented on the FPGA to cover the tile array. The number of tiles in a BISTER will depend on the number of tiles needed to implement the TPG and ORA logic. It is important to notice that the tiles which are dedicated to the TPG and ORA logic are not completely tested. In order to guarantee testing of all tiles, the FPGA will be reconfigured to shift the BISTERs across the entire array as shown in Fig. 4. Over the course of several reconfigurations, all tiles will be tested by acting as a BUT in a BISTER", fig. 4, page 1338, col. 2, paragraphs 3-4, Harris et al.).

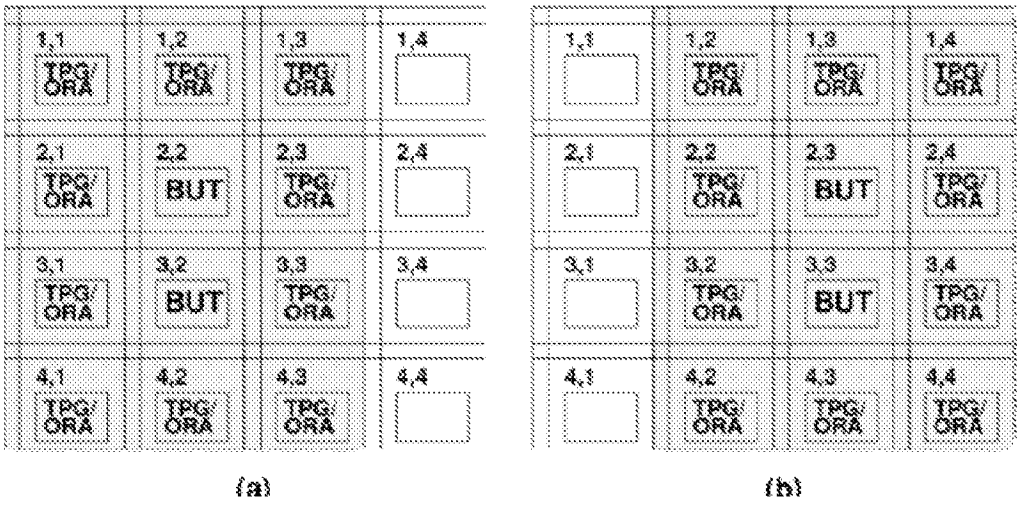

Fig. 4. Shifting BISTERs across FPGA array: (a) BISTER in lower left and (b) BISTER shifted right.

- As per claim 4, Harris et al. and Venkatesan teach the additional limitations.

Harris et al. teach configuring the second set and the fourth set to be third testing circuitry and fourth testing circuitry, respectively, and operating the second set and the fourth set to test the first set and the third set, respectively ("Each BISTER will be implemented as a rectangular block of tiles, and many BISTERs will be implemented on the FPGA to cover the tile array. The number of tiles in a BISTER will depend on the number of tiles needed to implement the TPG and ORA logic. It is important to notice that the tiles which are dedicated to the TPG and ORA logic are not completely tested. In order to guarantee testing of all tiles, the FPGA will be reconfigured to shift the BISTERs across the entire array as shown in

Fig. 4. Over the course of several reconfigurations, all tiles will be tested by acting as a BUT in a BISTER", page 1338, col. 2, paragraphs 3-4, Harris et al.).

- As per claim 5, Harris et al. and Venkatesan teach the additional limitations.

Harris et al. teach the step of configuring the first set includes: configuring N > 1 configurable logic blocks of the first set to operate as an N-bit input generator; and coupling an output of the N-bit input generator to the configurable logic blocks of the second set ("In each configuration, FPGA circuitry dedicated as BIST logic will perform test generation and response analysis to test non-BIST FPGA circuitry. To accomplish BIST, we use the test structure presented in [10] in which the FPGA is configured as many independent BISTER's structures, shown in Fig. 3. Each BISTER is composed of a test pattern generator (TPG), an output response analyzer (ORA), and two blocks under test (BUTs). The TPG is simply a counter which applies an exhaustive test sequence to the BUTs. Each BUT is a single tile in the FPGA which is being tested. The ORA is a comparator which sets the Pass/Fail flip-flop to "1" if the outputs of both BUTs do not agree. Each BISTER will be implemented as a rectangular block of tiles, and many BISTERs will be implemented on the FPGA to cover the tile array. The number of tiles in a BISTER will depend on the number of tiles needed to implement the TPG and ORA logic", Page 1338, col. 2, paragraphs 2-3, Harris et al.).

- As per claim 6, Harris et al. and Venkatesan teach the additional limitations.

Harris et al. teach a step of configuring a configurable logic block of the first set to determine whether the N-bit input generator outputs a predetermined value ("Each BISTER is composed of a test pattern generator (TPG), an output response analyzer (ORA), and two blocks under test (BUTs). The TPG is simply a counter which applies an exhaustive test sequence to the BUTs", page 1338, col. 2, paragraph 3, Harris et al.). The examiner would like to point out that the maximum value of the counter (TPG) is a predetermined value.

- As per claim 7, Harris et al. and Venkatesan teach the additional limitations.

Harris et al. teach that the step of configuring the N > 1 configurable logic blocks includes configuring the N> 1 configurable logic blocks to operate as an N-bit counter ("Each BISTER is composed of a test pattern generator (TPG), an output response analyzer (ORA), and two blocks under test (BUTs). The

TPG is simply a counter which applies an exhaustive test sequence to the BUTs. Each BISTER will be implemented as a rectangular block of tiles, and many BISTERs will be implemented on the FPGA to cover the tile array. The number of tiles in a BISTER will depend on the number of tiles needed to implement the TPG and ORA logic", page 1338, col. 2, paragraph 3, Harris et al.).

- As per claim 8, Harris et al. and Venkatesan teach the additional limitations.

Harris et al. teach that the predetermined value is a maximum value of the N-bit counter ("Each BISTER is composed of a test pattern generator (TPG), an output response analyzer (ORA), and two blocks under test (BUTs). The TPG is simply a counter which applies an exhaustive test sequence to the BUTs", page 1338, col. 2, paragraph 3, Harris et al.).

- As per claim 10, Harris et al. and Venkatesan teach the additional limitations.

Harris et al. teach that the verifier is configured to accept the N-bit input, and wherein each of the M groups includes N-1 configurable logic blocks configured to supply N-1 bits to the verifier ("Each BISTER is composed of a test pattern generator (TPG), an output response analyzer (ORA), and two blocks under test (BUTs). The TPG is simply a counter which applies an exhaustive test sequence to the BUTs. Each BUT is a single tile in the FPGA which is being tested. The ORA is a comparator which sets the Pass/Fail flip-flop to "1" if the outputs of both BUTs do not agree. Each BISTER will be implemented as a rectangular block of tiles, and many BISTERs will be implemented on the FPGA to cover the tile array. The number of tiles in a BISTER will depend on the number of tiles needed to implement the TPG and ORA logic", Page 1338, col. 2, paragraph 3, Harris et al.).

- As per claim 12, Harris et al. and Venkatesan teach the additional limitations.

Harris et al. teach the step of configuring the verifier includes configuring the verifier to deterministically output a failure indicator ("Each BISTER is composed of a test pattern generator (TPG), an output response analyzer (ORA), and two blocks under test (BUTs). The TPG is simply a counter which applies an exhaustive test sequence to the BUTs. Each BUT is a single tile in the FPGA which is being tested. The ORA is a comparator which sets the Pass/Fail flip-flop to "1" if the outputs of both BUTs do not agree", Page 1338, col. 2, paragraph 3, Harris et al.).

6. Claims 13, 14, 15, 16, 17, 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Butts et al. (US 5,036,473) in view of Cote et al. (US 6,470,485 B1) and Fluegge (US 5,745,372).

As per claim 13, Butts et al. teach configuring a first routing portion to map N inputs of the first routing portion to N outputs of the first routing portion in a first configuration; the N inputs of the second routing portion configured to be coupled to the N outputs of the first routing portion; applying input data to the inputs of the first routing portion; and receiving output data from the output of the second routing portion, the output data being responsive to the input data (fig. 3, col. 2, lines 15-19, col. 11, lines 46-50, col. 12, lines 30-37, col. 13, lines 5-35, Butts et al.).

However Butts et al. do not explicitly teach the specific use of a method of testing routing portions in an emulation system.

Cote et al. in an analogous art teach that the ability of all parts of the interconnect within the IC…proper operation of the integrated circuit (col. 1, lines 59-64, Cote et al.). Cote et al. also teach that testing of interconnect resources…fully operational (col. 2, lines 16-27, Cote et al.). Cote et al. teach that a simulation model of the FPGA under-test is constructed with its logic blocks configured to implement sequencers such as shown in FIG. 2A (col. 13, lines 18-20, Cote et al.). Cote et al. teach to efficiently test all of the diversified interconnect resources of the FPGA embodiment 300 (fig. 3A, col. 18, lines 58-60, Cote et al.). Cote et al. teach test-enabling reconfigurations of the FPGA 300…interconnect is free of defects (col. 19, lines 28-60, Cote et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Butts et al.'s patent with the teachings of Cote et al. by including an additional step of using the method of testing routing portions in an emulation system.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the method of testing routing portions in an emulation system would provide the opportunity to verify that all parts of the interconnect within the IC correctly and consistently route all signals in timely and accurate fashion between configurable logic blocks.

Butts et al. also do not explicitly teach the specific use of configuring a second routing portion to map N inputs of the second routing portion to N outputs of the second routing portion in a second configuration inverse to the first configuration.

Fluegge in an analogous art teaches that when a signal must go from a PALE circuit in a tile of one LEAF of one BLOCK of one SECTOR to a PALE circuit of a tile within another SECTOR, the signal must traverse through a level zero wire, then to a level one wire, then to a level two wire, then to a level three wire, and then to a level four wire, so that it can span to the other SECTOR. Once the signal reaches the other SECTOR, it must reverse this route from the level four wire in that SECTOR, down to a level three wire, down to a level two wire, then down to a level one wire, and finally down to a level zero wire so that it can enter the logic circuitry 302 in the new location (fig. 3, col. 5, lines 5-16, Fluegge).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Butts et al.'s patent with the teachings of Fluegge by including an additional step of configuring a second routing portion to map N inputs of the second routing portion to N outputs of the second routing portion in a second configuration inverse to the first configuration.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide required routing of signals to the system elements.

- As per claim 14, Butts et al., Cote et al. and Fluegge teach the additional limitations.

Cote et al. teach the method, further comprising a step of determining whether a difference exists between the input data and the output data (fig. 3A, col. 19, lines 57-60, Cote et al.).

- As per claim 15, Butts et al., Cote et al. and Fluegge teach the additional limitations.

Cote et al. teach the method, further comprising a step of configuring a first group of configurable logic blocks to perform the step of applying, wherein the configurable logic blocks include logic circuitry for implementing reprogrammable logic (fig. 1B, col. 5, lines 47-48, Cote et al.).

- As per claim 16, Butts et al., Cote et al. and Fluegge teach the additional limitations.

Cote et al. teach the method, further comprising a step of configuring a second group of configurable logic blocks to perform the step of determining (col. 9, lines 44-46, Cote et al.).

- As per claim 17, Butts et al., Cote et al. and Fluegge teach the additional limitations.

Cote et al. teach the method, wherein the N inputs of the second routing portion are configured to be coupled to the N outputs of the first routing portion through at least one reconfigurable interconnect (fig. 1B, col. 7, lines 2-8, Cote al.).

- As per claim 23, Butts et al., Cote et al. and Fluegge teach the additional limitations.

Butts et al. teach an integrated circuit, comprising: a first routing portion configured to map N inputs of the first routing portion to N outputs of the first routing portion in a first configuration, and configured to receive input data; wherein the N inputs of the second routing portion are coupled to the N outputs of the first routing portion (fig. 3, col. 2, lines 15-19, col. 11, lines 46-50, col. 12, lines 30-37, col. 13, lines 5-35, Butts et al.).

Fluegge teaches a second routing portion configured to map N inputs of the second routing portion to N outputs of the second routing portion in a second configuration inverse to the first configuration, and configured to output data (fig. 3, col. 5, lines 5-16, Fluegge).

Cote et al. teach monitoring logic configured to determining whether a difference exists between the input data and the output data (fig. 3A, col. 19, lines 57-60, Cote et al.).

7. Claims 18-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al. (Testing and Diagnosis of Interconnect Faults in Cluster-based FPGA Architectures, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 21, Issue 11, November 2002, Pages 1337-1343) in view of Takagi et al. (US 5,436,559).

As per claim 18, Harris et al. teach an integrated circuit, comprising: a first set of configurable logic blocks; a second set of configurable logic blocks, coupled to the first set; wherein the first set is further configured to provide an N-bit input generator to the second set and to provide a configurable logic block, separate from the N-bit input generator, as a verifier to verify the output data of the second set ("In each configuration, FPGA circuitry dedicated as BIST logic will perform test generation and response analysis to test non-BIST FPGA circuitry. To accomplish BIST, we use the test structure presented in [10] in which the FPGA is configured as many independent BISTER's structures, shown in Fig. 3. Each BISTER is composed of a test pattern generator (TPG), an output response analyzer (ORA), and two blocks under

test (BUTs). The TPG is simply a counter which applies an exhaustive test sequence to the BUTs. Each BUT is a single tile in the FPGA which is being tested. The ORA is a comparator which sets the Pass/Fail flip-flop to "1" if the outputs of both BUTs do not agree. Each BISTER will be implemented as a rectangular block of tiles, and many BISTERs will be implemented on the FPGA to cover the tile array. The number of tiles in a BISTER will depend on the number of tiles needed to implement the TPG and ORA logic", fig. 3, page 1338, col. 2, paragraphs 2-3, Harris et al.).

However Harris et al. do not teach a data processing portion coupled to the first set, the data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, and the second set is configured to output data in response to the second test pattern received from the first set.

Takagi et al. in an analogous art teach that FIG. 1 is a conceptional diagram of functional test of a semiconductor device, particularly a semiconductor integrated circuit device. Referring to FIG. 1, a testing apparatus includes a pattern generator 500 for generating a test pattern, a test pattern applying apparatus 501 for receiving the test pattern from pattern generator 500, to convert the received test pattern into logic signals of logical one or logical zero and apply the signals to an input terminal 510 of a device 502 under test, an output pattern discriminating circuit 504 for receiving an output signal from device 502 under test (fig. 1, col. 1, lines 48-58, Takagi et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Harris et al.'s publication with the teachings of Takagi et al. by including an additional step of a data processing portion coupled to the first set, the data processing portion configured to provide a first test pattern to the first set, wherein the first set is configured to provide a second test pattern to test the second set, and the second set is configured to output data in response to the second test pattern received from the first set.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to generate test pattern to test a logic block using an input test pattern from a data processing system.

- As per claim 19, Harris et al. and Takagi et al. teach the additional limitations.

Harris et al. teach the integrated circuit, wherein the first set is further configured to compare the output data to predetermined output data ("In this paper, an FPGA fault test and diagnosis approach is described that performs built-in self-test (BIST) on a cluster-based FPGA device. During the testing process, a portion of the FPGA is configured as test generation and response circuitry for a cluster under test", page 1337, col. 2, paragraph 3, Harris et al.).

- As per claim 20, Harris et al. and Takagi et al. teach the additional limitations.

Takagi et al. teach the data processing portion is further configured to provide a third test pattern to the second set, the second set is further configured to provide a fourth test pattern to test the first set, and the first set is further configured to output second data in response to fourth test pattern received from the second set (fig. 1, col. 1, lines 48-58, Takagi et al.).

8. Claim 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Harris et al. (Testing and Diagnosis of Interconnect Faults in Cluster-based FPGA Architectures, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 21, Issue 11, November 2002, Pages 1337-1343) and Takagi et al. (US 5,436,559) as applied to claim 18 above, and further in view of Venkatesan (Modelling Feedback Control Adjustment to Control Output Product Quality, Proceedings of American Control Conference, May 2002, vol. 6, Pages 5049-5053).

As per claim 22, Harris et al. and Takagi et al. substantially teach the claimed invention described in claim 18 (as rejected above). Takagi et al. further teach that the output of the verifier is a failure indicator ("Device 560 carries out a certain operation in accordance with the applied input test pattern and outputs an output signal indicating results of the operation as an output response pattern. Comparator 557 included in testing apparatus 551 compares the output response pattern from device 560 with the expected output pattern stored in memory 556. If this expected output pattern matches the output response pattern, then it is determined that device 560 operates normally. Conversely, if the expected output pattern mismatches the output response pattern, then it determined that there is a failure in device 560", col. 2, lines 35-47, Takagi et al.).

However Harris et al. and Takagi et al. do not explicitly teach that that an output of the verifier is an input to the verifier.

Venkatesan in an analogous art teaches that this paper describes a method to model feedback control adjustment to control the quality of products at the output of a continuous process (abstract, Venkatesan).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Harris et al.'s publication with the teachings of Venkatesan by including additionally that an output of the verifier is an input to the verifier.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to keep a steady output value of the failure indicator.

9. Claim 24 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (US 5,903,744) in view of Harris et al. (Testing and Diagnosis of Interconnect Faults in Cluster-based FPGA Architectures, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Volume 21, Issue 11, November 2002, Pages 1337-1343) and Takagi et al. (US 5,436,559).

As per claim 24, Tseng et al. teach an emulation system, comprising: a plurality of emulation boards; and a plurality of interconnect boards interconnecting the plurality of emulation boards (fig. 1, col. 1, line 51-col. 2, line 16, Tseng et al.).

However Tseng et al. do not explicitly teach the specifically that each of the plurality of interconnect boards has an integrated circuit having first and second sets of configurable logic blocks.

Harris et al. in an analogous art teach an island-style FPGA architecture which is composed of an array of identical tiles as shown in fig. 1(a). Each tile is composed of a cluster and surrounding interconnect. Each cluster is composed of a set of basic logic elements (BLE), each of which is composed of a set of programmable lookup tables (LUT), multiplexers, and flip-flops (page 1338, col. 1, paragraph 4, 6, Harris et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tseng's patent with the teachings of Harris et al. by including additionally that each of the plurality of interconnect boards has an integrated circuit having first and second sets of configurable logic blocks.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to build integrated circuits with reconfigurable logic.

Tseng et al. also do not explicitly teach a data processing portion coupled to the first and second sets, wherein the data processing portion is configured to provide a first test pattern to the first set to test the second set and a second test pattern to the second set to test the first set.

However Takagi et al. in an analogous art teach that FIG. 1 is a conceptional diagram of functional test of a semiconductor device, particularly a semiconductor integrated circuit device. Referring to FIG. 1, a testing apparatus includes a pattern generator 500 for generating a test pattern, a test pattern applying apparatus 501 for receiving the test pattern from pattern generator 500, to convert the received test pattern into logic signals of logical one or logical zero and apply the signals to an input terminal 510 of a device 502 under test, an output pattern discriminating circuit 504 for receiving an output signal from device 502 under test (fig. 1, col. 1, lines 48-58, Takagi et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tseng's patent with the teachings of Takagi et al. by including a data processing portion coupled to the first and second sets, wherein the data processing portion is configured to provide a first test pattern to the first set to test the second set and a second test pattern to the second set to test the first set.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to generate test pattern to test a logic block using an input test pattern from a data processing system.

10. Claim 25 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tseng et al. (US 5,903,744) in view of Butts et al. (US 5,036,473), Cote et al. (US 6,470,485 B1) and Fluegge (US 5,745,372).

As per claim 25, Tseng et al. teach an emulation system, comprising: a plurality of emulation boards; and a plurality of interconnect boards interconnecting the plurality of emulation boards (fig. 1, col. 1, line 51-col. 2, line 16, Tseng et al.).

However Tseng et al. do not explicitly teach specifically that each of the plurality of interconnect boards has an integrated circuit having first and second routing portions, wherein the first routing portion is configured receive input data and to map N inputs of the first routing portion to N outputs of the first routing portion in a first manner, wherein the second routing portion is configured to output data.

Butts et al. in an analogous art teach that logic chips…realized logic (col. 11, lines 46-50, Butts et al.). Butts et al. also teach that route the interconnections…accomplish the interconnect (col. 12, lines 30-37, Butts et al.). Butts et al. teach that the channel-routing interconnect…alternating logic and routing chips (col. 13, lines 6-27, Butts et al.). Butts et al. also teach that an "interconnect chip" is an electronically reconfigurable device which can implement arbitrary interconnections among its I/O pins. A "routing chip" is an interconnect chip used in a direct or channel-routing interconnect (col. 2, lines 15-19, Butts et al.).06

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tseng's patent with the teachings of Butts et al. by including additionally that each of the plurality of interconnect boards has an integrated circuit having first and second routing portions, wherein the first routing portion is configured receive input data and to map N inputs of the first routing portion to N outputs of the first routing portion in a first manner, wherein the second routing portion is configured to output data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to route signals in the interconnect boards so that the emulation boards can be interconnected.

Tseng et al. also do not explicitly teach specifically that the monitoring logic is configured to determining whether a difference exists between the input data and the output data.

However Cote et al. in an analogous art teaches that eight independent feedback paths…free of defects (fig. 3A, col. 19, lines 57-60, Cote et al.).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tseng's patent with the teachings of Cote et al. by including additionally that the monitoring logic is configured to determining whether a difference exists between the input data and the output data.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to find defects in the interconnect so that the signals can be routed correctly using a fault-free interconnect.

Tseng et al. also do not explicitly teach specifically that the second routing portion is configured to map N inputs of the second routing portion to N outputs of the second routing portion in a second manner inverse to the first manner.

However Fluegge in an analogous art teaches that when a signal must go from a PALE circuit in a tile of one LEAF of one BLOCK of one SECTOR to a PALE circuit of a tile within another SECTOR, the signal must traverse through a level zero wire, then to a level one wire, then to a level two wire, then to a level three wire, and then to a level four wire, so that it can span to the other SECTOR. Once the signal reaches the other SECTOR, it must reverse this route from the level four wire in that SECTOR, down to a level three wire, down to a level two wire, then down to a level one wire, and finally down to a level zero wire so that it can enter the logic circuitry 302 in the new location (fig. 3, col. 5, lines 5-16, Fluegge).

Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Tseng's patent with the teachings of Fluegge by including additionally that the second routing portion is configured to map N inputs of the second routing portion to N outputs of the second routing portion in a second manner inverse to the first manner.

This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that it would provide the opportunity to provide required routing of signals to the system elements.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DIPAKKUMAR GANDHI whose telephone number is (571)272-3822. The examiner can normally be reached on 9:00 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on (571) 272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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